ABSTRACT OF THE DISCLOSURE

A method of manufacturing a twin-ONO-type SONOS memory using a reverse self-alignment process, wherein an ONO dielectric layer is formed under a gate and physically separated into two portions using a reverse self-alignment process irrespective of photolithographic limits. To facilitate the reverse self-alignment, a buffer layer and spacers for defining the width of the ONO dielectric layer are adopted. Thus, the dispersion of trapped charges during programming and erasing can be appropriately adjusted, thus improving the characteristics of the SONOS. The present invention prevents the redistribution of charges in time after the programming and erasing operations.